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| Implementation of a DC-coupled CMOS Amplifier |
| ECSE 330 – Introduction to Electronics |
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***Abstract—*One of the fundamental purposes of analog electronics is connecting generic voltage (or current) sources that have standardized parameters with devices that have particular input range requirements. Therefore, it is necessary to develop cost-efficient amplifier circuits that take the source signal and alter it to satisfy the loading device input range. In this particular design problem, a 50 mV AC signal from a transducer is passed through a CMOS amplifier, which is coupled with a 17 V power supply, to be inputted into a microcontroller ADC port that only accepts signals between 2 – 6 V. In order to successfully and accurately (i.e. no signal loss) amplify the signal an AC gain of 20 V/V and a DC bias of 4 V were chosen to keep the ADC input voltage between approximately 3 – 5 V. This design was successful in assuring that the amplified output was well within the specified 2 – 6 V constraint and that all design specifications were implemented. However, due to the component values chosen to build the amplifier, and the inherent limitations of estimating, the amplifier output signal ended up being constrained between 3.35 – 4.65 V, rather than the expected range of 3 – 5 V.**

1. INTRODUCTION

The purpose of this experiment was to design a DC-coupled CMOS circuit that would amplify signals from a transducer with a peak-to-peak value of 100 mV over a frequency range of 100 to 10,000 Hz. The amplified signal was to be connected to the ADC port of a microcontroller. The ADC input port only accepted signals in the range of 2 – 6 V and the input resistance and capacitance of the ADC port were 1 MΩ and 10 pF, respectively. The CMOS amplifier was to be coupled with a DC Voltage of 17 V (*VO*). By building a common-source NMOS amplifier and coupling it with a power supply that has a DC output voltage of 17 V, it was possible to implement these specifications and amplify the transducer signal to be compatible with the acceptable ADC input port input voltage range.

1. CALCULATION OF POWER SUPPLY DC OUTPUT

The required power supply DC output voltage was derived as such (ID Number – 260365970):

(1)

(2)

The output of the power supply is 17 V.

1. POWER SUPPLY CALCULATIONS

The power supply was sourced by a 60 Hz 169.7 V AC signal. It needed to be able to provide a DC coupling voltage of 17 V to the NMOS Amplifier. Therefore, it was necessary to set compatible component values to the transformer inductors (*Lp*, *Ls*), filtering capacitor (*C*), current limiting resistor (*R*1), source resistor (*Rso*), and zener diode voltage (*Voz*) and resistor (*rz*) that made up the power supply. Other values, such as the source voltage (*vac*), the rectifier diode (D1N4148) and the zener diode component diodes (Dreverse, Dforward) were provided from the beginning. The set-up of these components can be observed in Figure 1.

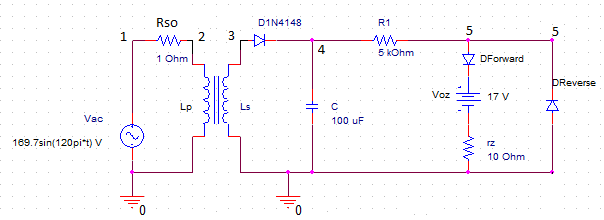


Fig. 1. Power Supply Circuit Diagram

*Rso* was chosen to be 1 Ω so that the voltage drop across the source resistor would be minimal and more voltage would be dropped across the inductor.

*VZO* was given a design value of 17 V. Due to the fact that in an accurate practical scenario that models the breakdown region of the zener diode, *IZ* and *IZK* will be very similar, *VZ* and *VZO* can be estimated to be equivalent. *VZ*, the voltage across the zener diode, will be the output voltage of the power supply (as they are in parallel). Thus, *VZO* should be assigned a value of 17 V.

The zener diode resistance, *rZ*, was chosen to be 10 Ω. One of the design specifications was that the power supply load regulation had to be greater than -5 mV/mA. The load regulation is equal to –*rZ*.Therefore, *rZ* must be greater than 5 *Ω*. A value of 10 *Ω* was therefore approximated for *rZ*.

Once *rZ* had been approximated, the power supply line regulation condition could be used to derive an acceptable value for *R*1. The line regulation, which must be less than 10 mV/V, can be represented by the ratio:

(3)

By manipulation of (3), it is clear that:

(4)

When *rZ* is equal to 10 *Ω,* as previously decided, *R*1 must be greater than 990 *Ω.* Thus, *R*1 was subsequently assigned a value of 5000 *Ω* in the design.

At this point it was necessary to pick inductor values for *Lp* and *Ls* that would influence a transformer secondary voltage (*vs*) with an amplitude close to 17 V*.* Having *VZO* be close to the amplitude of *vs* would decrease the variation from *VZO* when calculating the non-loaded output voltage of the power supply. In order to simplify calculations, inductor values of 70 mH for *Lp* and 1 mH for *Ls* were chosen. Using the equation:

(5)

It can be shown the amplitude of *vs* will be equal to roughly 20.28 V

It was also necessary to choose an acceptable nominal source AC ripple voltage (*Vr*). In order to maintain accuracy, but keep the system stable, .05 V was estimated as an acceptable nominal AC ripple voltage, *Vr*. Using the formula

(6)

it could be shown that the filtering capacitance needed in order to safely achieve this nominal AC ripple voltage, was approximately 108 µF. In order to keep component values standard (and therefore costs low), however, a capacitance of 100 µF was chosen for the filter. Flipping (6) to calculate the new nominal AC ripple voltage yielded *Vr* = .055 V.

The nominal source DC voltage (*V+*|*nominal*) could now be derived from the nominal AC ripple voltage:

(7)

This calculation resulted in *V+*|*nominal* ≈ 20.26 V.

Using *V+*|*nominal* and *Vr*, it was possible to calculate the unloaded (*VO,no-load*) and loaded (*VO*) output voltages of the power supply using:

(8)

(9)

Solving these equations, *VO,no-load* = 17.0066 V and *VO* = 17.0017 V. Although these are not perfect approximations of 17 V, the error is less than .1% in both cases, and the difference could safely be ignored. (Note: the load for the loaded output voltage was based on the input resistance of the amplifier circuit, which will be derived in Section V).

1. AMPLIFIER CALCULATIONS

In order to design the CMOS Amplifier, four resistances (*Rg1*, *Rg2*, *Rd*, *Rs*) and two capacitances (*Cc1*, *Cs*) needed to be chosen. The transducer source signal was a 50 mV AC signal over a frequency range of 100 to 10,000 Hz and the load resistance and load capacitance corresponding to the ADC input port were 1 MΩ and 10 pF, respectively. This information can be seen in Fig. 2.

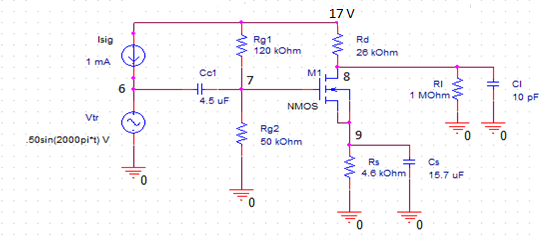


Fig. 2. Amplifier Circuit Diagram

In order to ensure that the amplified input signal would be within the specified 2 – 6 V accepted range, a 3 – 5 V target range was designated for the amplified signal. This was to guard against unstable fluctuations in the amplified voltage. This decision would entail a 1 V AC signal and a 4 V DC Bias. Therefore, the AC gain, *Av*, could be calculated to be 1V/50mV = 20 V/V. Because the DC bias for the amplified signal would be 4 V, the drain voltage of the NMOS Amplifier, *VD*, would also be 4 V. *VDD*, the DC coupling provided by the power supply, was approximately 17 V. Using the relational equation

(10)

it could be calculated that the Overdrive Voltage, *VOV*, is equal to 1.3 V. With this value, and the equations *VOV* = *VG* – *VS* – *Vt* and *VGD* ≤ *Vt*, it was concluded that *Vg* must be less than 5.4 V. These equations are by-products of the NMOS saturation condition; a condition that is necessary for the input signal to be amplified. Therefore, *VG* (the gate voltage) was assigned the value of 5 V. Using the overdrive voltage relation mentioned above, it could be derived that *VS*, the NMOS source voltage, is 2.3 V.

Now that *VG* had been designated as 5 V, a relationship between the resistors, *Rg1* and *Rg2* could be quickly calculated using a voltage divider. In order to keep component values simple but within design specifications (i.e. Amplifier input resistance > 20 kΩ; Maximum Resistor Value ≤ 10 MΩ), the values *Rg1* = 120 kΩ and *Rg2* = 50 kΩ were chosen.

Based on *VOV* and the NMOS design characteristic, *Kn* = .6mA/V2, the drain current, *iD*, could be solved for using the equation:

(11)

which resulted in *iD* being approximately equal to .51 mA. Using *iD*, and the relationships:

(12) (13)

*RD* and *Rs* could be calculated to be approximately 26 kΩ and 4.6 kΩ, respectively.

Finally, using these resistor values, the capacitances *Cc1* and *Cs* could be derived using:

(14) (15)

Where (16)

*Cc1* was equal to 4.5 µF and *Cs* was equal to 15.7 µF.

After solving a small signal model to calculate the AC component of the output voltage, it is found that *vL* ≈ -.936 V indicating that the expected amplifier output signal range is approximately 3.064 V – 4.936 V.

1. SIMULATION RESULTS

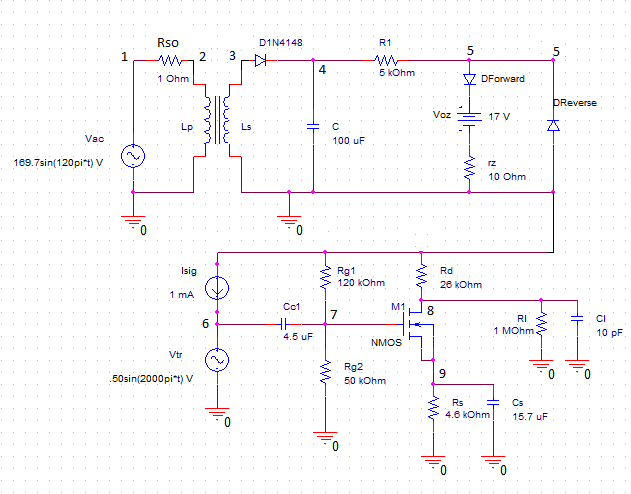


Fig. 3. Full System Circuit

After simulating the system with the given and derived component values in SPICE (see NetList in appendix C), the transient response of the output voltage of the power supply (i.e. the DC coupling voltage) turned out to be almost exactly the same as the expected transient response. (Note: the plots show the power supply voltage results when it is loaded with the amplifier circuit as seen in Fig. 3).

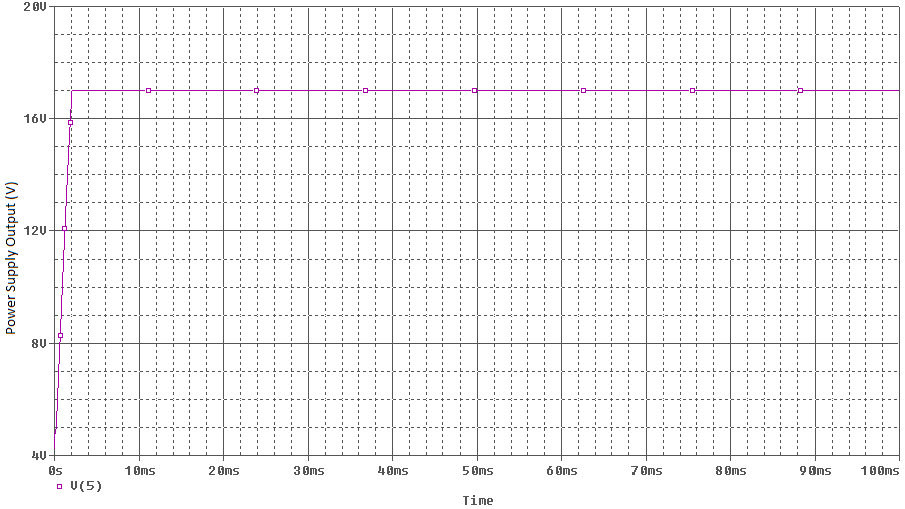


Fig. 4. Power Supply Output Voltage

As expected and seen in Fig. 4, the power supply voltage quickly rose to around 17 V and stabilizes at that value for the remainder of the simulation.

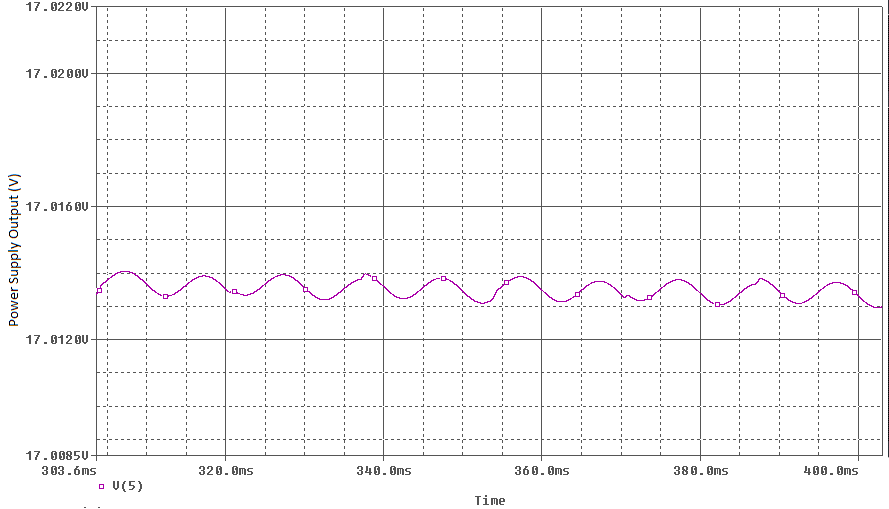


Fig. 5. Power Suppy Output Voltage Magnified

However, if the power supply output voltage is magnified, it can be seen that the average power supply output voltage is not exactly at 17 V, and is in fact at a voltage that is higher than the expected loaded output voltage of around 17.0017 V. The observed average output voltage for the loaded power supply in Fig. 5 was around 17.0135 V. This difference corresponded to a less than .07% error with the expected loaded voltage, and a less than .08% error with ideal value of 17 V. Thus, it could largely be ignored. The circuit components chosen for the power supply adequately modeled the final expected behavior of the power supply.

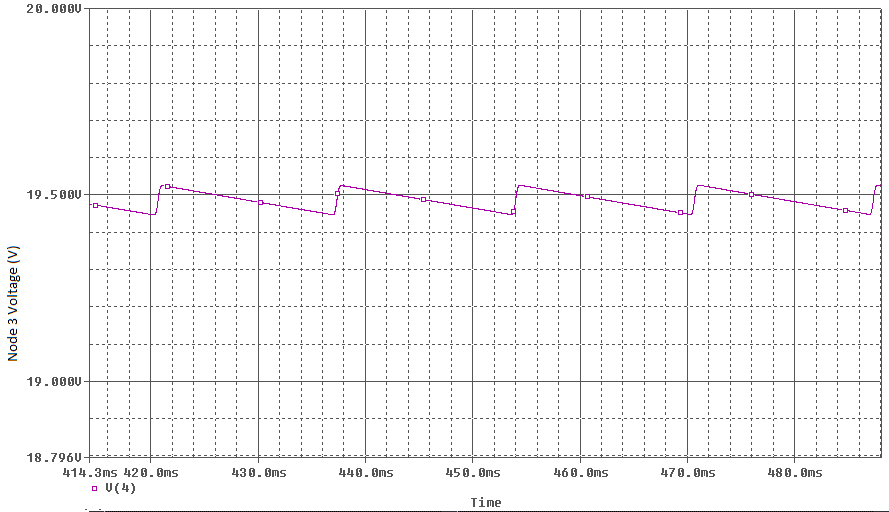


Fig. 6. Nominal AC Ripple Voltage Magnified

Although the final behavior of the power supply was correctly modeled by the chosen component values, the internal behavior was not as accurate. A nominal AC ripple voltage of approximately .055 V was expected based on the calculations done in (6) with C = 100 µF. Fig. 6, however, suggests that the nominal AC ripple voltage is closer to .075 V, which would correspond to an error of more than 36%. Similarly, the nominal source DC voltage is closer to 19.49 V. It was expected to be around 20.26 V. This corresponds to an error of 3.8%. However, due to inverse relationship between *V+*|*nominal* and *Vr* derived in depicted in (7), it follows that if *Vr* is greater than expected, *V+*|*nominal* will be less than expected. These values complement one another.

The voltage output of the entire system exhibited the transient response that was expected (see Fig. 7). The output voltage initially rises as the DC coupling voltage is transferred directly to the load. Then as the source voltage, *Vs*, of the NMOS amplifier begins to rise, the output voltage is damped, and it eventually stabilizes to a range in between 2 – 6 Volts, which is exactly what the system design required. (Note: All output plots were simulated with the test diagram in Fig. 3)

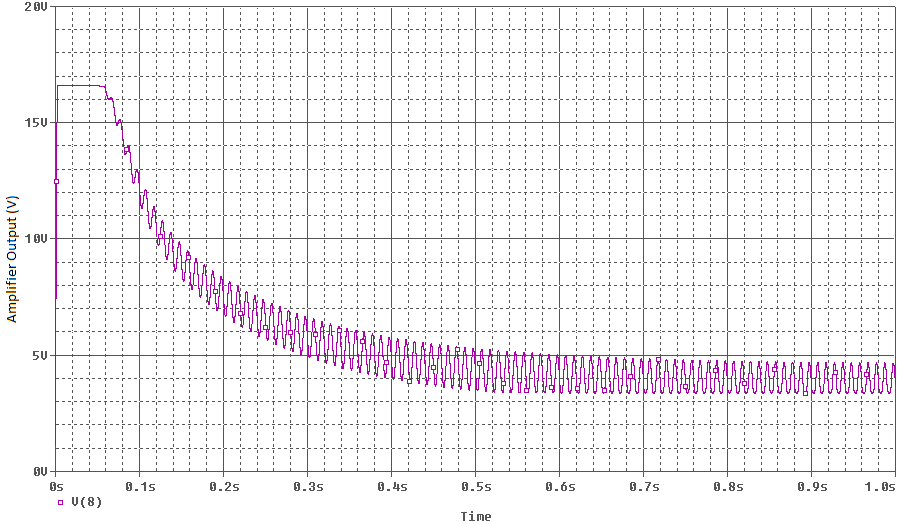


Fig. 7. System Output

Upon closer inspection of the amplified signal, however, as seen in Fig. 8, it is observed that the signal does not match the expected output range. The predictive calculations had estimated that the output range of the entire system would be between 3.064 – 4.936 V. This range is clearly not reached. The signal seems to fluctuate between 3.35 – 4.65 V once it stabilizes. Because the DC bias is the same for both ranges, the difference in range corresponds to an AC error of approximately 31%. This discrepancy is most likely caused by the fact that all capacitors are assumed to be shorted in the small signal model used in the calculations. However, because the capacitors have finite capacitances, there will be an AC voltage drop across them due to their impedances.

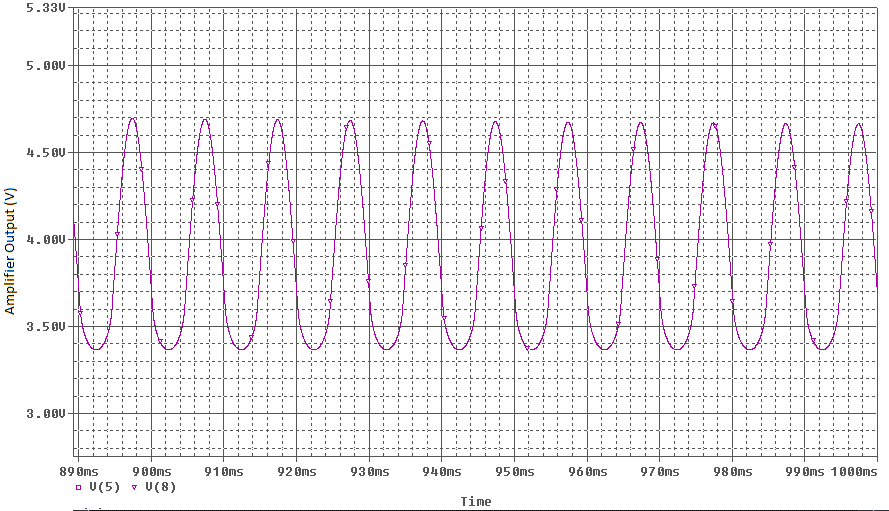


Fig. 8. Magnified System Output

The capacitors are also responsible for the band-pass nature of the frequency response, as they set the lower cut-off frequency of the filter. Although the frequency response does not match up perfectly with what the amplifier bandwidth specification stated (i.e. 100 Hz – 10 kHz), it would not filter out any signals from the transducer because the filter bandwidth is wider (i.e. 10 Hz – 1 MHz as seen in Fig. 9) than the transducer frequency range (i.e. 100 Hz – 10 kHz). Unfortunately, the ADC input port will be subject to more noise at lower and higher frequencies because those signals (i.e. 10 Hz – 100 Hz, 10 kHz – 100 kHz) will be able to pass through even when the amplifier should have filtered them out.

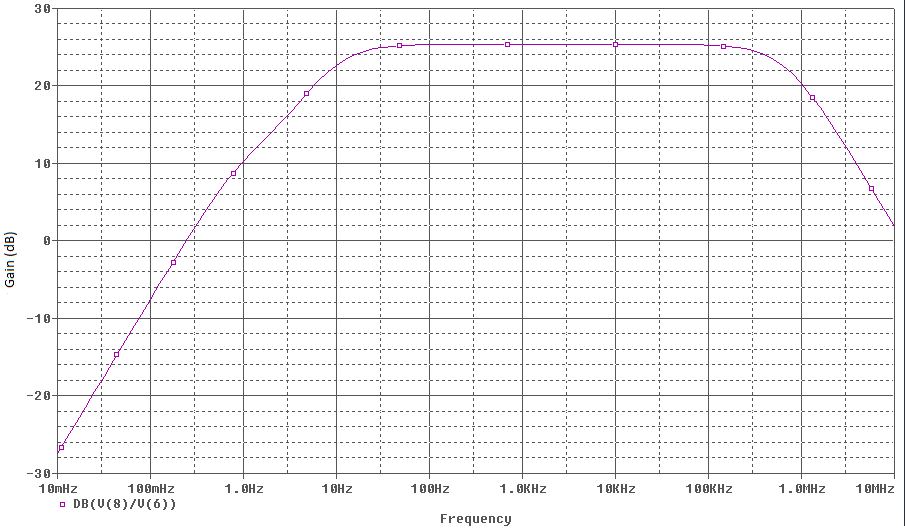


Fig. 9. Frequency Response of System

In the case of the upper limit of the filter, this cannot be helped. The upper limit of the band-pass filter is dictated by internal capacitors of the MOSFET. They cannot be changed, so the ADC input port would be exposed to those high frequencies anyway. The lower cut-off frequency of the filter could be shifted to a higher frequency by decreasing the capacitance of *Cs*. This, however, would cause the amplifier gain (*gm)* to decrease due to (12). This is not desired as the gain is already less than expected.

1. CONCLUSION

Although the results from the simulation sometimes differed from the results expected from the calculations, the design still clearly works. Despite discrepancies with the internal voltages of the power supply, the overall behavior of the power supply as seen from an external load will be almost equal to the calculated value, and very close to the ideal 17 V.

For the amplifier, there may have been error between the expected output values and the actual output values, but the actual output values still satisfy the specifications. The system output voltage range, 3.35 – 4.65 V, will always be between 2 – 6 Volts once it stabilizes, so there will be no losses due to the signal amplitude. And all frequencies between 100 Hz and 10 kHz, which is the range of the transducer, are within the band-pass area of the frequency response of the system, so there will be no loss due to transducer frequencies that are too low or too high.

1. APPENDICES

Appendix A: SPICE Netlist

\* SPICE MODEL

\*DC-Coupled CMOS Amplifier

\*zener diode subcircuit

.subckt zener\_diode 1 4

Dforward 1 2 Dideal

Dreverse 4 1 1mA\_diode

VZ0 2 3 DC 17V

Rz 3 4 10

\*diode model statements

.model 1mA\_diode D (Is=100pA n=1.679)

.ends zener\_diode

\*\* Main Circuit \*\*

\* ac line voltage

Vac 1 0 sin(0 169.7V 60Hz)

Rso 1 2 1

\*Transformer

Lp 2 0 70mH

Ls 3 0 1mH

K12 Lp Ls .999999

\*Rectifier diode

D1 3 4 D1N4148

\*Filter and Voltage Regulator

C 4 0 100u

R1 4 5 5000

XZ1 5 0 zener\_diode

\*Amplifier

\*Signal Components

Isig 6 5 DC 1m

Vtr 6 0 AC 1 sin(0 .05V 100 0 0)

Cc1 6 7 4.5u

\*Gate Resistances

Rg1 5 7 120k

Rg2 7 0 50k

\*Drain Components

Rd 5 8 26k

\*NMOS Source Components

Rs 9 0 4600

Cs 9 0 15.7u

\*NMOS Amplifier

M1 8 7 9 9 nnMOS L=10u W=10u

\*Load Components

Rl 8 0 1e6

Cl 8 0 10p

\* CD4007 Discrete NMOS & PMOS

.model nnMOS NMOS (LEVEL=2 VTo=1.4 Kp=.6m LAMBDA=0.005)

\* Ideal Diode Model

.model Dideal D (Is=100pA n=0.01 )

\*

\* D14148 Rectifier Diode

.model D1N4148 D (Is=5.84n N=1.94 Rs=.7017 Ikf=44.17m Xti=3 Eg=1.11 Cjo=.95p M=.55 Vj=.75 Fc=.5 Isr=11.07n Nr=2.088 Bv=100 Ibv=100u Tt=11.07n)

\*

\* CD4007 Discrete NMOS & PMOS

\*Analysis Requests

.OPTIONS ITL5 = 0

.TRAN .01ms 1s 0 .01ms UIC

.AC DEC 10 .01 10Meg

.plot TRAN V(5,0)

.PROBE

.end

**Appendix B**: Higher Resolution Simulation Plots

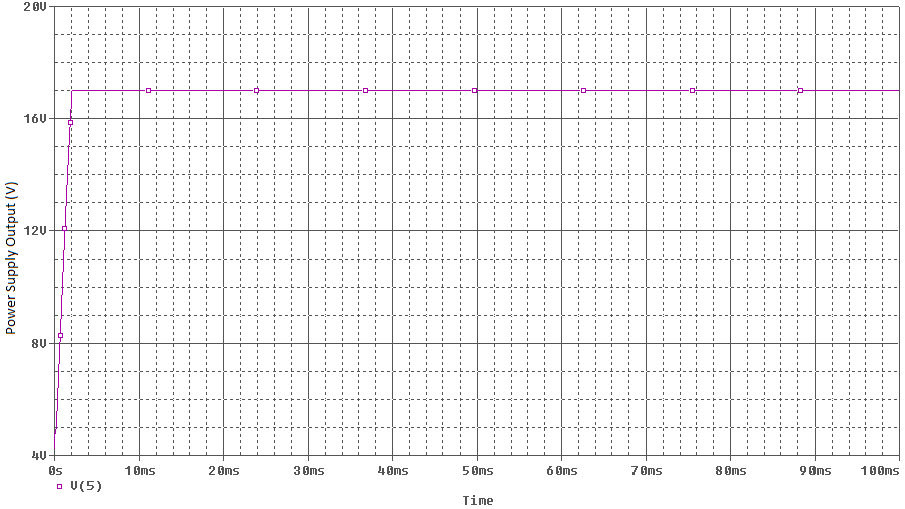


Fig. A. Transient Response for Power Supply Output Voltage

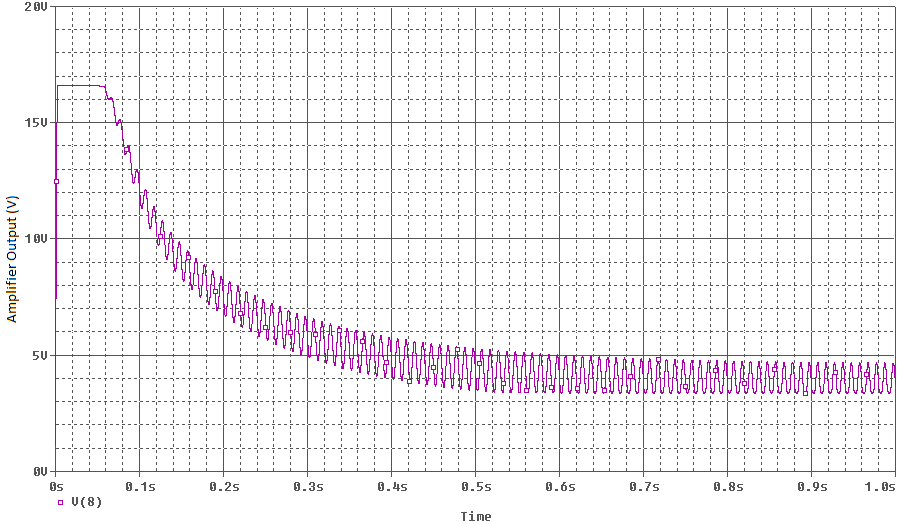


Fig. B. Transient Response of Complete System

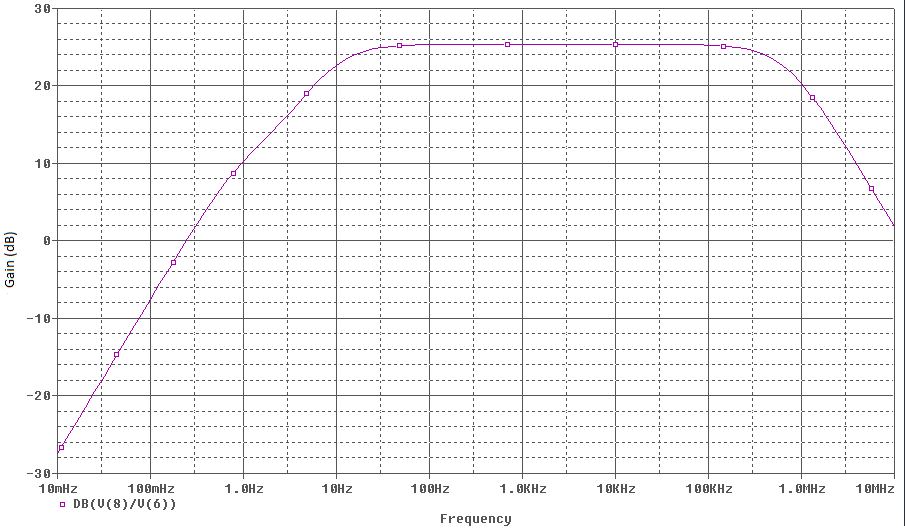


Fig. C. Frequency Response of System

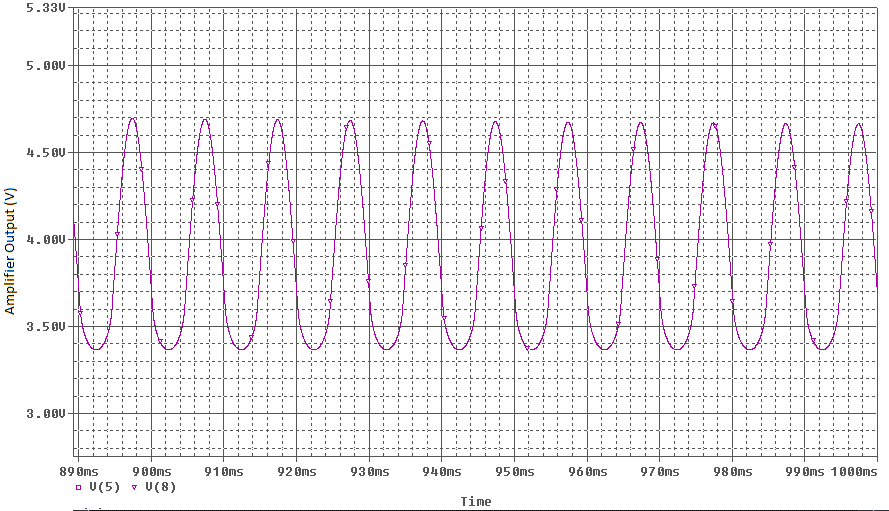


Fig. D. Magnified Amplifier Output

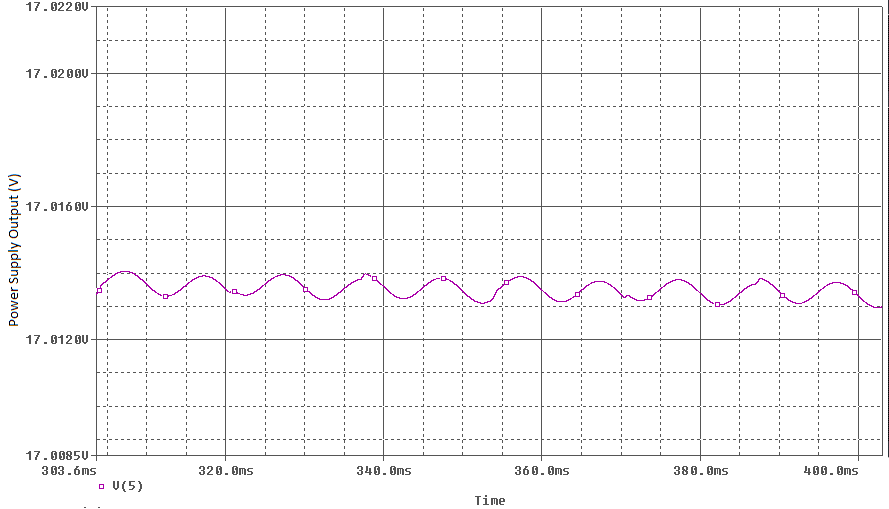


Fig. E. Magnified Power Supply Output

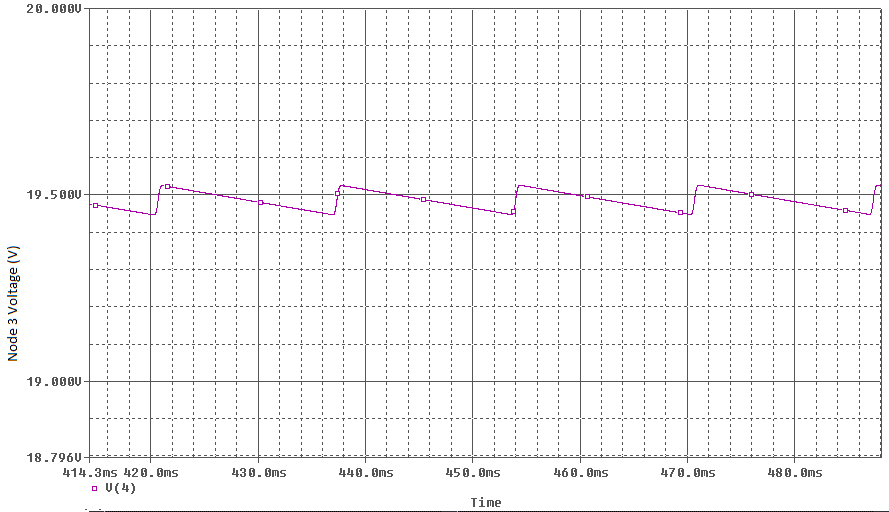


Fig. F. Nominal Source AC Ripple Voltage

**Appendix C**: Circuit Diagram

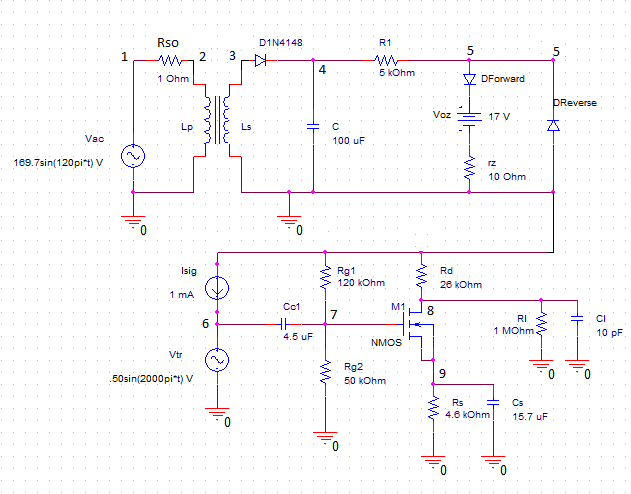


Fig. i. Circuit Diagram of Systems

1. VARIABLE TABLES

Power Supply:

|  |  |  |
| --- | --- | --- |
| Variable | Representation | Value |
| Source Voltage | *vac* | 169.7sin(120πt) |
| Source Resistance | *Rso* | 1 Ω |
| Left Transformer Inductor | *Lp* | 70 mH |
| Right Transformer Inductor | *Ls* | 1 mH |
| Filtering Capacitor | *C* | 100 µF |
| Current-Limiting Resistor | *R*1 | 5 kΩ |
| Zener Diode Voltage | *VZO* | 17 V |
| Zener Diode Resistance | *rZ* | 10 Ω |

Amplifier:

|  |  |  |
| --- | --- | --- |
| Variable | Representation | Value |
| Transducer Voltage | *vtr* | .05sin(2000πt)\* |
| Coupling Capacitance 1 | *Cc1* | 4.5 µF |
| Gate Resistance 1 | *Rg1* | 120 kΩ |
| Gate Resistance 2 | *Rg2* | 50 kΩ |
| Drain Resistance | *RD* | 26 kΩ |
| Source Resistance | *RS* | 4.6 kΩ |
| Source Capacitance | *Cs* | 15.7 µF |
| Load Resistance | *RL* | 1 MΩ |
| Load Capacitance | *CL* | 10 pF |

\*For the purposes of the simulation

1. REFERENCES

[1] G. W. Roberts. *Introduction to Electronics.* Montreal: McGill University, 2012.

[2] G.W. Roberts. “Prof. Gordon W. Roberts.” Internet: http://www.ece.mcgill.ca/~grober4, [April 5, 2012]

[3] G. W. Roberts and A. S. Sedra. *SPICE*. New York: Oxford University Press, Inc., 1997, pp. 82 – 95.